Successful Alloy Attachment of GaAs MMIC's

JEANNE S. PAVIO

Abstract—Alloy attachment of GaAs monolithic circuits was examined after initial reflow, after environmental bake, and after a stepped series of thermal cycles from 200 to 1000 cycles (−55 to +125°C). The variety of solders tested included both pastes and preforms. Monolithic assemblies alloyed with these solders were evaluated for changes in physical properties as well as for changes in electrical performance. It was noted during the study that via fractures due to thermal expansion differences between the alloy and the GaAs monolithic device were a common occurrence and could become an inherent reliability risk. Based on this evidence, an investigation relating the frequency of fracturing to the size and the shape of the vias was undertaken. Results led to the development of processing parameters which could minimize and control fracture occurrence.

I. Introduction

ALLOY ATTACHMENT of GaAs MMIC's is presented utilizing a reflow operation for attachment of multiple devices simultaneously rather than manual scrub of each monolithic sequentially. Reflow characteristics of a variety of solders were analyzed as well as the behavior of those solders during long-term temperature bake and during 1000 cycles of thermal cycle. RF and thermal impedance data were measured through 600 thermal cycles in order to verify long-term electrical performance. Finally, the study addressed fractures in GaAs due to thermal expansion differences between the alloy and the GaAs MMIC itself. The main objective for the monolithic attachment study was to identify alloy materials and to develop processes which provide the following characteristics:

- reliability
- reworkability
- ease of processing and repair
- mechanical accuracy
- electrical stability.

Initially a broad variety of alloys were examined both in solder pastes and in preform configuration. These were then reduced to four alloys: Pb/Sn/Ag (90/5/5), Pb/In/Ag (92.5/5/2.5), Pb/In (75/25), and Au/Sn (80/20). The monolithic circuit utilized for the evaluation was a power chip with dimensions of 0.098 in ×0.081 in with gold backside metallization, and both vias and air bridges (Fig. 1).

Manuscript received April 30, 1987; revised September 8, 1987. This work was supported in part by the Naval Research Laboratory, Washington, DC 20375, under Contract N00014-84-C-2057, CLIN 0002AA, Sequence B0001.

The author is with Texas Instruments Inc., Dallas, TX 75265.

IEEE Log Number 8717681.

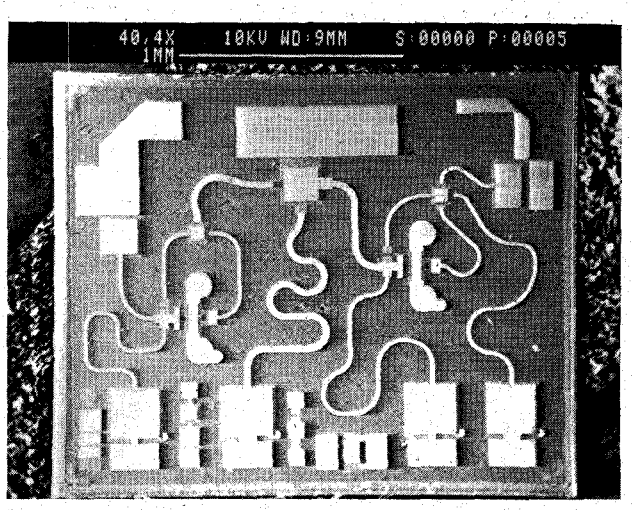


Fig. 1. Test device.

The test cycle was separated into two phases. The first phase included investigation of physical properties of the attachment media such as voiding, wetting, intermetallic formation, and fracture behavior. The second phase examined process and electrical characteristics such as processing ease and repairability, tolerance of movement during reflow, sensitivity to cumulative effects of assembly flow, and changes in electrical performance (RF and thermal impedance) during long-term environmental testing.

The environmental cycle for each of the candidates included a bake of 150°C for 168 h. Samples were baked, examined microscopically, and microsectioned for detection of gold diffusion and fractures. Another group was then subjected to thermal cycling from −55 to +125°C for 1000 cycles. Samples for each solder were microsectioned initially and at 200-cycle intervals. These were than analyzed with the scanning electron microscope and energy dispersive X-ray. Colored maps were developed with the X-ray so that boundaries, macrostructures within the solder joint, and intermetallic characteristics were clearly visible.

II. Discussion

After furnace profile development, analysis of the alloy samples began with examination of wetting behavior and X-ray analysis used for measurement of voiding. Wetting characteristics and voiding are listed in Table I.

0018-9480/87/1200-1507$01.00

TABLE I
WETTING AND VOIDING CHARACTERISTICS

Solder Candidate	Paste/ Preform	Wetting	% Void Free Area
Au/Sn	preform	excellent	95%
Au/Sn	paste	very good	85%
Pb/Sn/Ag	preform	very good	90%
Pb/Sn/Ag	paste	excellent	85%
Pb/In/Ag	preform	good	85%
Pb/In/Ag	paste	very good	85%
Pb/In	preform	good	85%
Pb/In	paste	fair	85%

Fig. 2. Fracture at via site.

During preliminary investigation of the alloy samples, a fracturing problem was noted at the via sites on the monolithic device (Fig. 2). The phenomenon was first apparent during a manual alloy scrub of a monolithic power circuit into a thermkon base package (thermal coefficient of expansion 6.0 in/in °C) using a AuSn solder preform. Every device mounted exhibited some cracking at the via sites, and electrical yield was less than 25 percent at the time. Although most of the cracks were of the concentric ring configuration, in some instances cracks beginning at the via sites would propagate completely across the device or across a FET or capacitor, causing electrical failure. Fig. 3 is a photograph of a fracture which has propagated across a gate stripe on an electrically failed device. Troubleshooting of the power monolithic assembly clearly pointed to the fact that the frequency of the cracks could be increased with excessive heat during the scrub operation or excessive time at temperature. Since the manual operation was subject to operator variation, particularly with respect to time at peak temperature, a more controlled furnace reflow profile was developed to alloy these MMIC's to the package base. Although fracturing of this monolithic was not completely eliminated when utilizing AuSn solder, via cracking could be reduced to less than 5

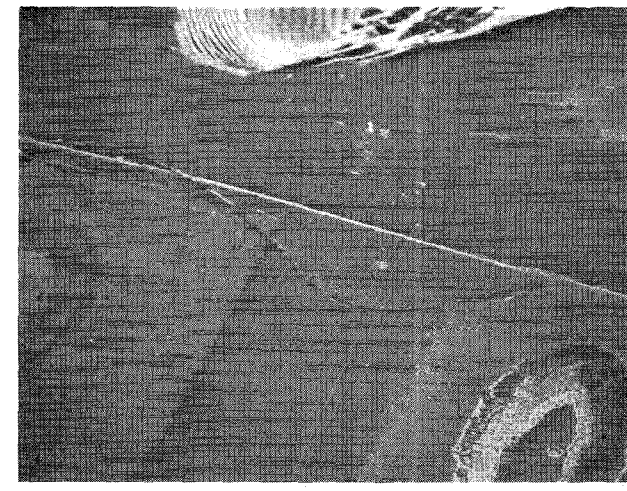


Fig. 3. Propagation across a gate stripe.

percent of the devices assembled when the peak temperature was lowered to the minimum heat required to reflow the alloy (310–320°C). Microsections, comparison of the fracture potential of this device with other monolithics reflowed at the same temperatures, and comparison of the frequency of cracking with alternative solder systems revealed some interesting results. Fractures at the via could be completely eliminated by utilization of a pliable solder such as those available in the indium-based systems. Unfortunately, due to the high oxidation potential of these alloys, repair work is difficult and usually results in a greater level of voiding on the repaired assembly than achievable with AuSn. Increased voiding is particularly deleterious to the electrical yield on a power monolithic assembly. Further investigation demonstrated that the fracture phenomenon was due to a thermal expansion mismatch between the GaAs (TCE 5.7×10^{-6} in/in°C) and the AuSn solder (TCE 16×10^{-6} in/in°C). Capillary action caused the vias to fill with solder and, in some cases, caused the alloy to pierce through the top surface of the device. It was found that the problem could be eliminated by limiting the amount of solder which penetrates the via. A critical process window must be developed for each alloy to minimize the amount of solder filling the via while at the same time maintaining sufficient backside solder coverage to provide good thermal dissipation.

From the broad variety of alloys examined initially, the candidates were narrowed to the four listed in Table I, and an environmental bake for 168 h at 150°C was completed. For the bake operation, four carrier plates per alloy, with six devices on each carrier plate, were reflowed, baked, and microsectioned. Environmental testing also encompassed thermal cycling. For these tests, 12 carrier plates per alloy were mounted with four MMIC's on each. Thermal cycling continued for a maximum of 1000 cycles, with two carrier plates for each solder sample pulled and microsectioned initially, and after 200-cycle interval steps.

The solder exhibiting the greatest change, due to thermal cycling, was Pb/Sn/Ag (90/5/5). After the initial reflow process, little gold plating remained either on the carrier

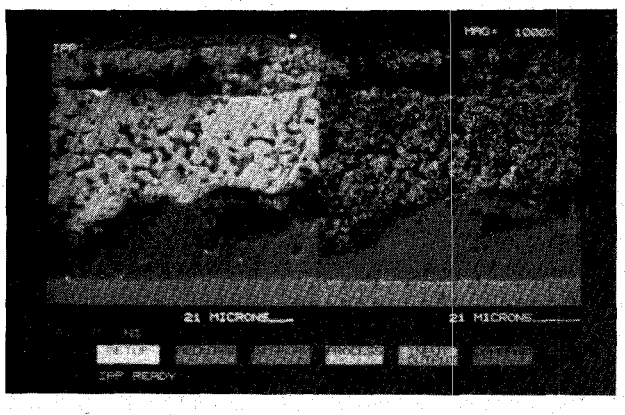


Fig. 4. Pb/Sn/Ag (90/5/5) gold diffused into solder and segregated into nuclei.

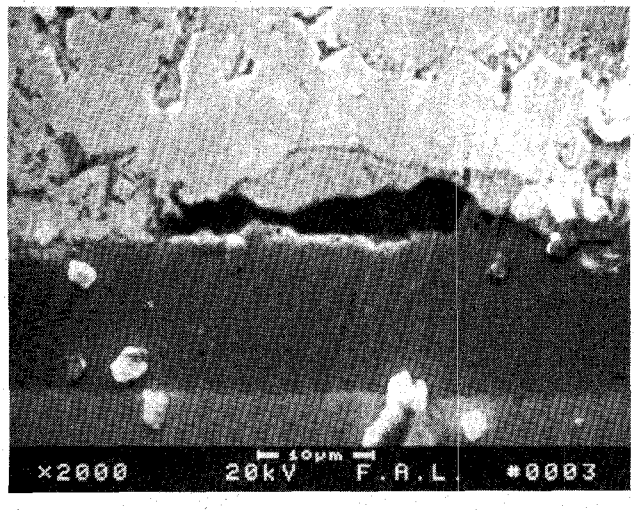
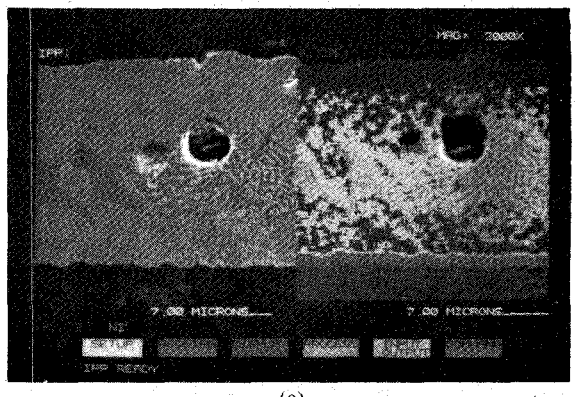


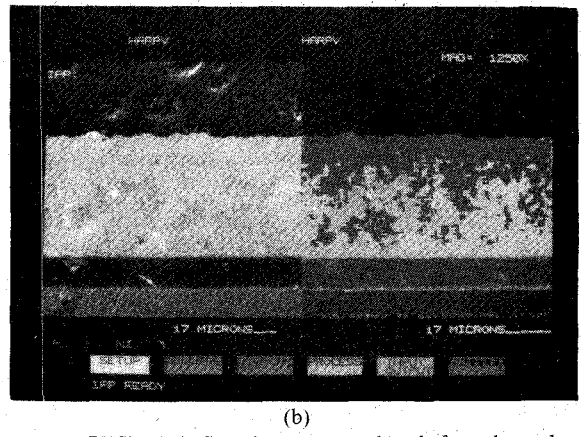
Fig. 5. Pb/In/Ag fractures in the gold-depleted region.

plate or on the underside of the MMIC. The gold had diffused into the solder and segregated into separate nuclei after the thermal cycling (Fig. 4). Pb/In/Ag (92.5/5/2.5) behaved in a similar fashion, with most of the gold diffusion occurring at initial reflow. Fractures began to occur at the gold/indium intermetallic boundaries within the solder joint and at the gold-depleted regions of both the carrier plate and the MMIC (Fig. 5).

Two candidates remained viable for MMIC attachment: Pb/In (75/25) and Au/Su (80/20). Fig. 6(a) and (b) compares energy dispersive X-ray maps and SEM's of a AuSn (80/20) solder joint microsection before and after thermal cycling (1000 cycles, −55°C to +125°C). The red area in the map is gold; the greatest concentration is found at the top and the bottom of the joint, near the base of the gold-plated monolithic and near the top of the carrier plate. The yellow area is the AuSn metallurgy of the alloy. Although additional gold has entered the solder joint during thermal cycling, particularly from the carrier plate, this has not led to fractures in the joint even after 1000 cycles. Likewise, Fig. 7(a) and (b) compares energy dispersive X-ray maps and SEM's of a PbIn (75/25) solder joint before and after thermal cycling (1000 cycles, −55°C to +125°C). The red once again depicts gold concentration;

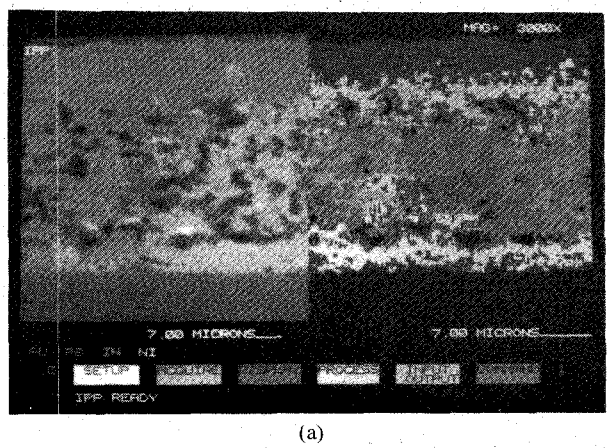


(a)

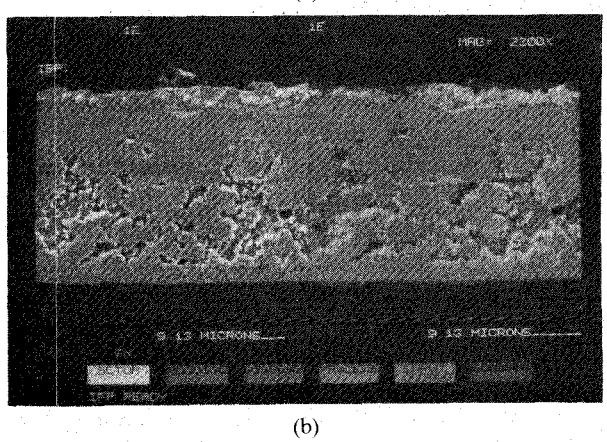


(b)

Fig. 6. (a) EDX of AuSn microsection taken before thermal cycling. (b) EDX of AuSn microsection taken after 1000 thermal cycles.



(a)



(b)

Fig. 7. (a) EDX of PbIn microsection taken before thermal cycling. (b) EDX of PbIn microsection taken after 1000 thermal cycles.

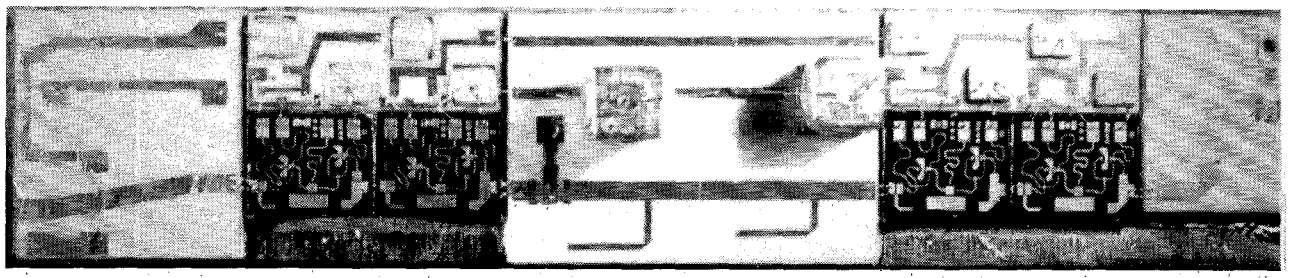


Fig. 8. Power amplifier assembly.

green is lead, and blue, indium. The pink area is an intermetallic of gold and indium while the lighter blue–green in the thermal-cycled sample is an indium intermetallic with lead. Initially, before cycling, the solder joint is separated into distinct layers. Proceeding from top to bottom, gold is visible entering the solder from the monolithic circuit backside. Next, there is a narrow band of gold/indium intermetallic followed by a narrow band of pure indium. The center of the solder joint contains a very wide band of almost pure lead. This is then followed by indium, indium/gold intermetallic, and gold from the carrier plate. After cycling, almost all of the gold, which diffused into the solder joint, has combined with indium. The indium has also formed more intermetallic with lead, and the center bond of lead has dispersed significantly through the width of the microsection. Small fractures are apparent in this lead, lead/indium area after thermal cycling. The fractures, however, have little depth and have not propagated even after 1000 cycles.

Both AuSn (80/20) and PbIn (75/25) have exhibited little gold diffusion into the solder joint when compared with the other candidate and minimal fractures which do not pose a reliability risk.

With the final candidates, 16 amplifiers were assembled and tested. Eight were tested for RF characteristics and eight for electrical thermal impedance characteristics. These were measured initially at 200, 400, and 600 cycles (thermal cycling from −55 to +125°C). No changes in RF performance or thermal impedance were experienced with either of the alloy samples. Fig. 8 shows the amplifier assembly which was completed on a gold plated molybdenum carrier plate.

III. Via Fracturing Evaluation

Although via fracturing had been minimized during the solder evaluation by strict control of peak temperature (310°–320°C), time at temperature (half minute), and ramp-down rate (15°–30° per minute), a low level of via fracturing was present in many monolithic assemblies even at the optimal heat profile. A GaAs test structure (Fig. 9) was designed incorporating variations in via size and shape. Slices were fabricated at two commonly utilized thickness levels, 4 mils and 6 mils. Devices were then reflowed, with AuSn solder, on a variety of carrier plates which are used for microwave monolithic assemblies. The gold pads, on the top surfaces of the monolithics, were then etched off in order to more clearly view any fractures which had developed at the vias during reflow. Tables II and III show the number of vias which exhibited cracks compared to the total number tested on 4-mil- and 6-mil-thick slices, respectively. Mask dimensions compared to actual via dimensions are shown in Table IV, which also shows the via test pattern. Overall results show a greater frequency of via cracking in the 6-mil-thick slice than in the 4-mil slice. A trend in both slices was that smaller dimension vias were less likely to crack than the large vias. The least amount of cracking was exhibited in the triangular vias, followed by the round vias. With the 4-mil-thick GaAs slice, no fractures were visible in the triangular vias; whereas in the 6-mil-thick slice, fracturing occurred in the 4.0-, 3.5-, and 3.0-mil (mask size) vias. No fracturing was apparent in the 2.5-mil vias and smaller.

Round vias, on the other hand, continued to fracture in the 4-mil-thick slice until the via diameter was reduced to 3.0 mils. With a 6-mil-thick slice, round vias continued to

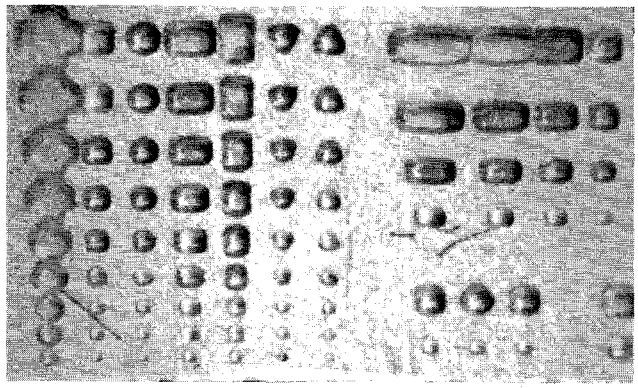


Fig. 9. GaAs via test device.

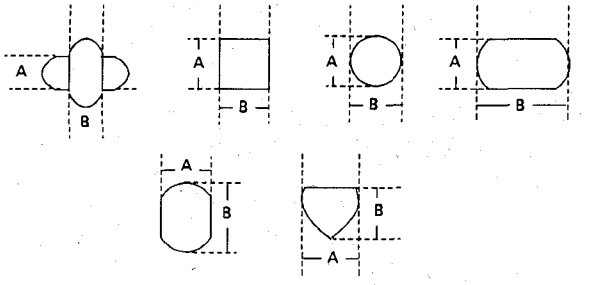
TABLE II
4-Mil-Thick GaAs Device: Via Cracking

Size mils	Clover Leaf		Square		Round		Oval (horiz)		Oval (vert)		Triangle	
	# Vias	%	# Vias	%	# Vias	%	# Vias	%	# Vias	%	# Vias	%
4.0	15/15	100	14/15	93	12/15	80	14/15	93	15/15	100	0/15	0
3.5	15/15	100	11/15	73	4/15	27	14/15	93	15/15	100	0/15	0
3.0	15/15	100	5/15	33	0/15	0	10/15	67	11/15	73	0/15	0
2.5	15/15	100	0/15	0	0/15	0	12/15	80	9/15	60	0/15	0
2.0	15/15	100	0/15	0	0/15	0	2/15	13	3/15	20	0/15	0
1.5	14/15	93	0/15	0	0/15	0	0/15	0	0/15	0	0/15	0
0.8	9/15	60	0/15	0	0/15	0	0/15	0	0/15	0	0/15	0
0.5	9/15	60	0/15	0	0/15	0	0/15	0	0/15	0	0/15	0

TABLE III
6-MIL-THICK GaAs DEVICE: VIA CRACKING

Size mils	Clover Leaf		Square		Round		Oval (horiz)		Oval (vert)		Triangle	
	# Vias	%	# Vias	%	# Vias	%	# Vias	%	# Vias	%	# Vias	%
4.0	15/15	100	15/15	100	11/15	73	15/15	100	14/15	93	11/15	73
3.5	15/15	100	14/15	93	11/15	73	12/15	80	12/15	80	3/15	20
3.0	15/15	100	10/15	33	5/15	33	13/15	87	10/15	33	1/15	7
2.5	15/15	100	7/15	47	3/15	20	10/15	33	8/15	42	0/15	0
2.0	15/15	100	1/15	7	0/15	0	8/15	53	10/15	33	0/15	0
1.5	14/15	93	0/15	0	0/15	0	1/15	7	1/15	7	0/15	0
0.8	11/15	73	0/15	0	0/15	0	0/15	0	0/15	0	0/15	0
0.5	11/15	73	0/15	0	0/15	0	0/15	0	0/15	0	0/15	0

TABLE IV
VIA DIMENSIONS: ACTUAL VERSUS MASK



Mask Size	Backside of Device Dimensions Actual Via Size (mils)											
A	A	B	A	B	A	B	A	B	A	B	A	B
4.0	9.7	9.8	9.0	8.4	8.7	8.8	9.7	14.0	9.7	13.5	8.3	7.7
3.5	8.8	8.5	8.4	8.3	8.2	8.2	8.7	12.2	9.0	12.4	7.8	7.3
3.0	8.1	7.8	7.8	7.7	7.5	7.6	8.1	11.2	8.3	10.9	6.9	6.5
2.5	6.8	7.3	6.7	7.0	6.7	6.9	7.2	9.9	7.3	9.6	6.0	5.9
2.0	6.2	6.0	6.0	6.2	5.6	6.0	6.4	8.4	6.6	8.2	5.2	5.0
1.5	5.4	5.8	5.2	4.9	5.0	4.8	5.8	7.4	5.6	7.2	4.8	4.2
0.8	3.8	4.3	3.8	4.2	3.7	4.2	4.2	5.5	4.5	5.2	3.6	3.7
0.5	3.4	3.3	3.5	3.4	3.5	3.7	3.9	5.0	4.3	4.8	3.2	3.2

Mask Size	Topside of Gold-Etched Device Actual Via Size (mils)											
A	A	B	A	B	A	B	A	B	A	B	A	B
4.0	7.5	9.6	7.2	8.1	6.2	7.1	8.6	13.4	10.3	11.8	5.2	4.3

fracture until the via diameter was reduced to 2.0 mils. The worst performer was the clover leaf via, which exhibited fracturing in all size categories. Although square vias fractured more readily than the round, square vias were overall better performers than the oval vias. As expected, the orientation of vias was not a factor in the incidence of via cracking with a vertical orientation compared to a horizontal orientation.

In the solder evaluation, it was seen that fractures emanating from the vias on a GaAs monolithic device exhibit configurations which are distinctly different from those resulting from handling damage. The fracturing is a reliability concern and can cause significantly lower yields, particularly on power circuits. It has been demonstrated that the frequency of fractures can be controlled by minimal heat and time at temperature during reflow (i.e., AuSn 310°–320°C for a half minute) or by the use of pliable solder systems. However, due to the high oxidation level incurred with many of these alloy systems, repair potential can become limited. Device fabrication variables which affect the cracking frequency are via size, shape, and slice thickness.

IV. CONCLUSIONS

In conclusion, an automated alloy attachment process was developed for GaAs MMIC's. The alloy materials analyzed included both pastes and performs. A comprehensive reliability evaluation demonstrated that even the mildest flux was not viable for application with GaAs MMIC's, and silver-bearing solders resulted in significant gold diffusion and fracturing during thermal cycling. Two viable candidates emerged from the test cycle, Au/Sn (80/20) and Pb/In (75/25). When examined electrically, amplifiers assembled with these candidates exhibited no change in thermal impedance or RF characteristics through 600 thermal cycles.

ACKNOWLEDGMENT

The author wishes to thank M. Wurtele of Texas Instruments, who was responsible for the design and implementation of the electrical test in this study.

Jeanne Pavio was born on July 6, 1949, in Fall River, MA. She received the bachelor of arts degree in 1971 and the M.S. degree in 1972, both from the University of Connecticut.

Since 1980 she has been employed at Texas Instruments in the Hybrid Microelectronics Laboratory and, for the past three years, in the Microwave Laboratory. Her experience has encompassed both thick- and thin-film hybrids and microwave components. Her current interests involve automated assembly and packaging of monolithic GaAs devices.